In the Specification

Please replace the paragraph at page 8, lines 13 through 16 with the following paragraph:

During cycle-slipping, sweeping of the VCO clock phases over the data stream causes the phase detector output V_{er} to oscillate between "early" and "late" signals. The frequency of this oscillation (sweep speed) is equal to the frequency difference between the receive clock and the incoming data.

Amendments to the specification are indicated in the attached "Marked Up Version of Amendments" (page i).

In the Claims

Please cancel Claims 14 and 29.

Please amend Claims 1, 2, 4, 11, 13, 17, 19, 26, 28, 30, 31 and 35. Amendments to the claims are indicated in the attached "Marked Up Version of Amendments" (pages i - v).

1.   (Amended) A frequency monitor, comprising:

an edge detector which produces an output comprising a pulse for each rising/falling edge of an error signal, the error signal having a frequency responsive to a difference between frequencies of two input signals;

a conductive circuit having an effective resistance depending on a rate of the edge detector output pulses;

a capacitor which holds a charge responsive to the effective average resistance of the conductive circuit; and

an indicator circuit which produces an output responsive to the charge held by the capacitor.

2.   (Amended) The frequency monitor of Claim 1, wherein the conductive circuit comprises: